

DEC 27 2005

App. No. 10/065,185

Response to Final Office Action mailed October 26, 2005

Page 2 of 5

R E M A R K S

Reconsideration of the present application in view of the following remarks is respectfully requested. Nine claims remain pending in the application: Claims 23 through 31, of which claim 31 is currently withdrawn as allegedly not being readable on the elected invention. Reconsideration of claims 23 through 30 in view of the remarks below is respectfully requested.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned at (858) 552-1311 so that such issues may be resolved as expeditiously as possible.

Claim Rejections - 35 U.S.C. § 102

1. Claims 23-30 stand rejected under 35 U.S.C. § 102(b), as being allegedly anticipated by U.S. Patent No. 6,282,583 (*Pincus et al.*).

As set forth at M.P.E.P. § 2131, a claim is anticipated only if every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Claim 23 is directed to a redundant bus controller (RBC). The claimed RBC includes, among other elements, "a peer coupling configured to communicate state information of the RBC to another bus controller" and "a sequencer configured to transition the state of the RBC."

The final office action suggests that the "multiple CPU registers provided in CPU register array 88" described in *Pincus*

App. No. 10/065,185

Response to Final Office Action mailed October 26, 2005

Page 3 of 5

et al. "define the redundant bus controllers." Further, the final office action apparently suggests that *Pincus et al.* teaches the claimed "peer coupling" because FIGS. 5 and 7 of *Pincus et al.* clearly show "each CPU 40... coupled to another CPU 40 ... and coupled to the ... register arrays 88" and that *Pincus et al.* teaches the claimed "sequencer" because *Pincus et al.* clearly teaches that the "sequencer 24 includes an array of CPU (i.e., processor registers) that are manipulated by the processing elements on the bus..."

Applicant respectfully submits, however, the fact that *Pincus et al.* clearly shows "that each CPU 40... coupled to another CPU 40 ... and coupled to the ... register arrays 88" or that *Pincus et al.* clearly teaches that the "sequencer 24 includes an array of CPU (i.e., processor registers) that are manipulated by the processing elements on the bus...", does not expressly or inherently suggest that *Pincus et al.* teaches or even suggests that either a peer coupling or sequencer are included within the "multiple CPU registers provided in CPU register array 88" that define RBC.

For example, FIG. 3 of *Pincus et al.* shows a plurality CPUs 40 connected to a sequencer 24 via bus 16. Similarly, FIG. 7 of *Pincus et al.* shows a plurality CPUs 40 connected to a CPU register array 88 via bus 66. However, the CPU register array 88 of *Pincus et al.* does not include a plurality of CPUs 40. Accordingly, whatever "peer coupling" allegedly taught by *Pincus et al.*, such a "peer coupling" is not included within the RBC (i.e., the "multiple CPU registers provided in CPU register array 88"). In fact, *Pincus et al.* discloses a peer coupling that is separate from such an RBC. Moreover, *Pincus et al.* fails to teach or suggest wherein any peer coupling is configured to

App. No. 10/065,185

Response to Final Office Action mailed October 26, 2005

Page 4 of 5

communicate state information of the RBC to another bus controller, as now recited in claim 23.

Moreover, *Pincus et al.* is silent as to any teaching or suggestion that the CPU register array 88 includes the sequencer 24. Indeed, the CPU register array 88 shown in FIG. 7 of *Pincus et al.* actually performs the function of the sequencer 24 (see *Pincus et al.*, col. 12, lines 28-30). Further, *Pincus et al.* is silent as to any teaching or suggestion that the sequencer 24 is configured to transition the state of the RBC (i.e., the "multiple CPU registers provided in CPU register array 88"), as now recited in claim 23.

For at least the reasons provided above, Applicant respectfully submits the present interpretation of *Pincus et al.* conflicts with the actual teachings of *Pincus et al.* Moreover, Applicant respectfully submits that *Pincus et al.* fails to describe, either expressly or inherently, each and every element now recited in claim 23. Accordingly, Applicant respectfully requests withdrawal of the present rejection under 35 U.S.C. § 102(b).

App. No. 10/065,185
Response to Final Office Action mailed October 26, 2005
Page 5 of 5

C O N C L U S I O N

Applicant submits that the above remarks place the pending claims in a condition for allowance. Therefore, a Notice of Allowance is respectfully requested.

Respectfully submitted,



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